

Appl. No. 09/992,387

Amdt. dated Feb.1, 2006

Reply to Office action of Nov. 3, 2005

Remarks/Arguments

Applicants thank Examiner Lewis again for her patient and careful examination of this application and her clear explanation of the claim rejections in the Office Action. Applicants respectfully submit, however, that because the cited reference does not disclose all the elements in the claims, it does not anticipate nor render the claims obvious and therefore the rejections are improper.

As presented, claim 25 describes a device that includes exit ports formed by vias that extend through the interposer. The claim further limits the device to have a bottom surface where the area immediately adjacent the exit ports being free of a conductive pattern and contact pad. The Miles patent does not disclose this limitation.

The Office Action refers to Figure 2 of the Miles patent as evidence that Miles discloses "the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad." But, contrarily, Figure 2 of the Miles patent clearly depicts a contact pad, designated by numeral reference 23, at the immediately adjacent surface of every exit port, and the Miles specification clearly describes this element 23:

Referring now to FIG. 2, it can be seen that the IC 10 lies over some of the conductive through holes 22 in the substrate. Each of these through holes 22 connects to a solder pad 23 on the bottom side of the substrate 16.¹

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The encapsulated package may now be placed onto a printed circuit board by any number of interconnection schemes. For example, the package may be attached to the circuit board by solder joints as in the C5 process (controlled-collapse-chip-carrier-connection). Or, it may be attached using elastomer interconnects or hot-melt adhesive interconnects. In the case of the C5 connections, solder balls 27 are bumped on the bottom of the substrate 16. When the chip carrier package is placed on the main circuit board, the solder balls are reflowed, providing electrical and mechanical contact between the package and the circuit board (not shown).²

The description clearly says that Fig. 2 depicts a solder pad 23 connected to each through-hole 22, and that there is a solder ball 27 on each solder pad 23, and the solder balls are reflowed to provide electrical and mechanical contact between the package and the circuit board.

¹ US 5,535,101, col. 4, ll. 7-10.

² Ibid., col. 4, ll. 56-67.

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Because the cited reference does not support the 103 rejection against claim 25, applicants respectfully submit that the rejection is improper. And claim 25 is not rendered by the reference and it stands patentable.

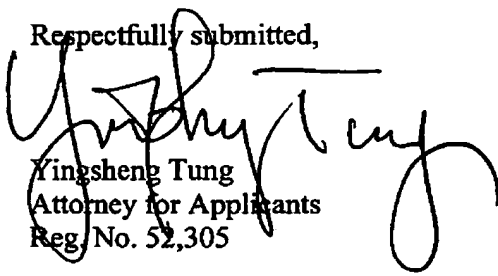
Claims 26 and 27 properly depend from patentable claim 25 and stand patentable at least by virtue of their dependence.

Claim 28 describes a substrate for connecting an integrated circuit chip. The substrate has a single-layered insulating interposer film through which vias are extended. The vias forms exit ports on the bottom surface of the substrate, the area immediately adjacent the exit ports is free of a conductive pattern and contact pad.

As presented relating to claim 25, the Miles patent does not disclose this limitation. The through-holes in the Miles patent are connected to the solder pads 23 on the bottom side of the substrate 16. Applicants respectfully submit that because the Miles patent does not disclose all the elements of limitation in claim 28, it does not anticipate claim 28 and the 102 rejection against claim 28 is improper, and claim 28 stands patentable over the Miles patent.

Claims 29-31 properly depend from patentable claim 28, they stand patentable at least by virtue of their dependence.

Respectfully submitted,


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